Third Semester B.E. Degree Examination, June/July 2018
Analog Electronics Circuits

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1 a. Assuming an ideal diode, sketch v_i, v_d and i_d for half-wave rectifier of Fig.1(a). The input is a sinusoid with frequency 50 Hz. **(08 Marks)**

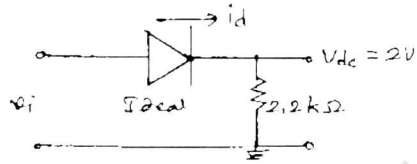


Fig.Q1(a)

b. Determine v_0 for the network shown in Fig.Q1(b). **(06 Marks)**

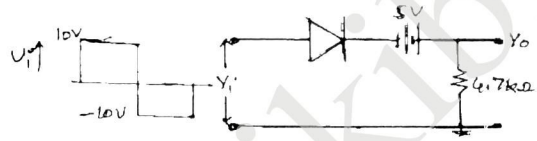


Fig.Q1(b)

c. Sketch v_0 for the network shown in Fig.Q1(c). **(06 Marks)**

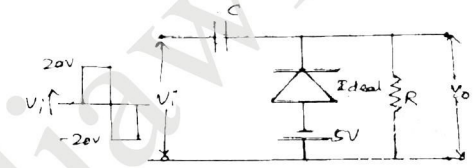


Fig.Q1(c)

2 a. Using exact analysis, obtain the Q-point values for the voltage-divider bias circuit. **(08 Marks)**

b. Obtain the expression for $S(I_{co})$ for an emitter-bias circuit and determine its value for the circuit with $R_B = 470\ k\Omega$, $R_E = 2.2k\Omega$, $R_C = 3.3k\Omega$, $V_{CC} = 12V$ and $\beta = 100$. **(06 Marks)**

c. For the circuit shown in Fig.Q2(c), determine the values for R_1 and R_C. **(06 Marks)**

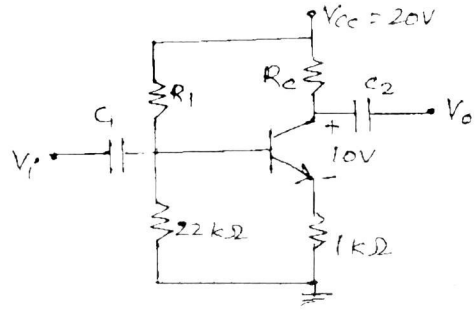


Fig.Q2(c)

3 a. Derive the equations for Z_i, Z_0 and A_V for fully by passed common emitter RC–coupled amplifier. **(08 Marks)**

b. Compare Z_i, Z_0 and A_V of a RC coupled amplifier with emitter follower and explain why emitter follower is called as impedance matching network. **(06 Marks)**

c. For the circuit shown in Fig.Q3(c), find Z_i, Z_0 and A_V. **(06 Marks)**

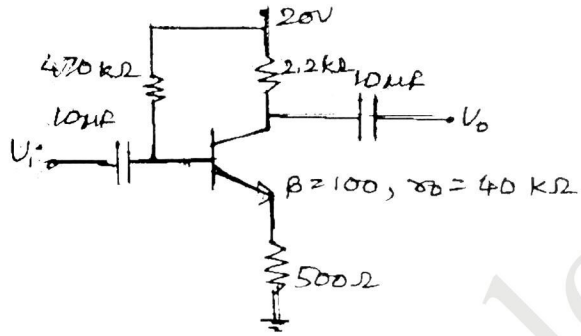


Fig.Q3(c)

4 a. Draw the frequency of RC coupled amplifier and explain high-pass action at low frequencies and low-pass action at high frequencies with relevant equations and Bode plots. **(08 Marks)**

b. Draw the high frequency equivalent circuit for RC coupled amplifier and obtain expressions for f_{H1} and f_{H0}. **(06 Marks)**

c. Determine f_{C_S} and f_{C_C} for circuit with,

$C_S = 10\mu F$, $C_E = 20\ \mu F$, $C_C = 1\ \mu F$, $R_S = 1k\Omega$, $R_1 = 40k\Omega$, $R_2 = 10\ k\Omega$, $R_E = 2k\Omega$, $R_C = 4k\Omega$, $R_L = 2.2k\Omega$, $\beta = 100$, $r_0 = \infty$, $V_{CC} = 20V$. **(06 Marks)**

PART – B

5 a. Explain the advantages of employing negative feedback in an amplifier. **(06 Marks)**

b. Derive an equation for Z_i and A_V for a Darlington emitter follower. **(08 Marks)**

c. For cascaded stages shown in Fig.Q5(c), determine :

i) Loaded gain for each stage

ii) Total gain for the system A_V and A_{VS}. **(06 Marks)**

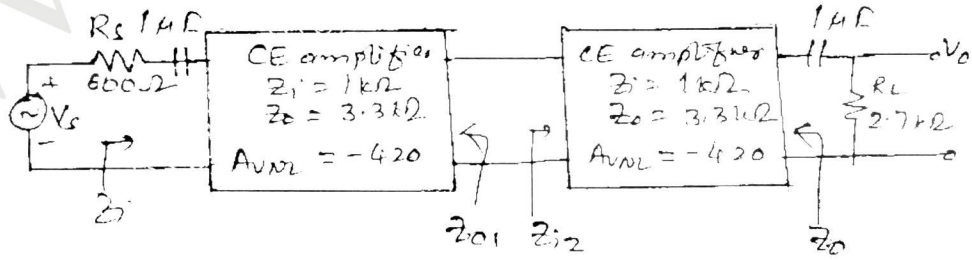


Fig.Q5(c)

6 a. Derive the expression for maximum percentage efficiency for a seriesfed class–A power amplifier. **(08 Marks)**

b. Calculate the second harmonic distortion for an output waveform with $V_{CE_Q} = 10V$, $V_{CE_{min}} = 1V$, $V_{CE_{max}} = 18V$. **(06 Marks)**

c. Draw the circuit of a class-B push-pull amplifier and explain the working. Explain why cross-over distortion occurs in class-B and how it is overcome. **(06 Marks)**

7 a. With a neat circuit diagram, explain the principle of operation of RC phase-shift oscillator with necessary equations. **(08 Marks)**

b. Explain the working of transistor crystal oscillator in series resonant mode. **(06 Marks)**

c. Design a Weinbridge oscillator for a frequency of 4KHz. **(06 Marks)**

8 a. Derive equations for Z_i, Z_0 and A_V for JFET fixed bias configuration, with source resistor bypassed. **(08 Marks)**

b. For JFET amplifier shown in Fig.Q8(b), find Z_i, Z_0 and A_V. **(08 Marks)**

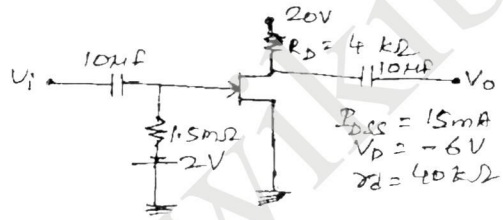


Fig.Q8(b)

c. Explain the graphical determination of g_m. **(04 Marks)**

Third Semester B.E. Degree Examination, June/July 2019
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat circuit diagram, explain Emitter stabilized bias circuit, write the necessary equation. **(08 Marks)**

b. Determine output voltage for the following circuit in Fig.Q.(b). Assume f = 1000Hz and ideal diode. **(06 Marks)**

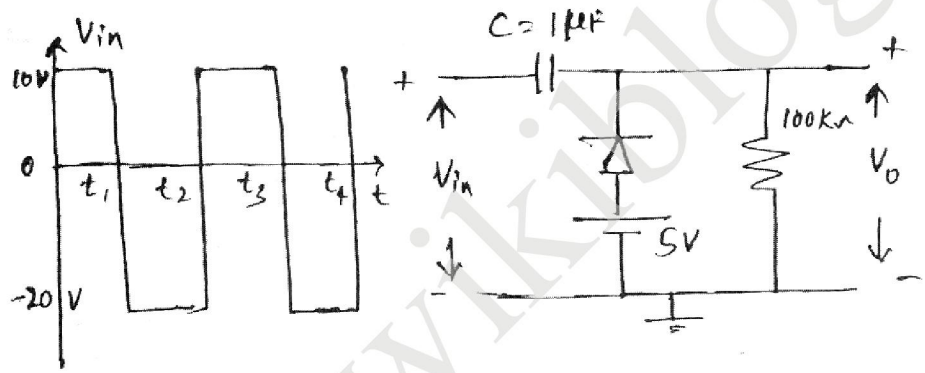


Fig.Q.1(b)

c. Derive the expression for stability factors of fixed bias circuit with respect to I_{CO}, V_{BE}, β and draw the circuit diagram. **(06 Marks)**

OR

2 a. Explain the circuit of a transistor switch being used as an inverter. **(06 Marks)**

b. Determine the voltage V_{CE} and the current I_C for the voltage divider configuration Given: $R_1 = 39K\Omega$, $R_2 = 3.9K\Omega$, $R_C = 10K\Omega$, $R_E = 1.5K\Omega$, $C_E = 50\mu F$, B = 100, $V_{BE} = 0.7$. **(08 Marks)**

c. Sketch the output waveform for the network shown in Fig.Q.2(c). If the peak value of the a.c input if 15V and draw the transfer characteristics. **(06 Marks)**

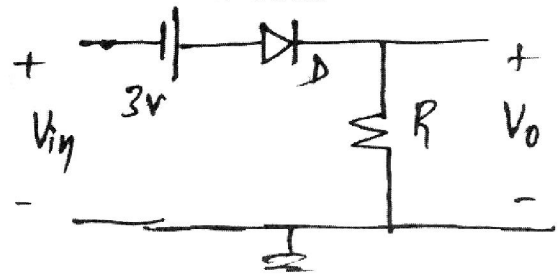


Fig.Q.2(c)

Module-2

3 a. With a neat circuit diagram, derive an expression for Z_i, Z_o and A_v of fixed bias circuit using r_e – model. **(08 Marks)**

b. For the Emitter follower network shown in Fig.Q.3(b). Determine r_e, Z_i, Z_o and A_v. **(06 Marks)**

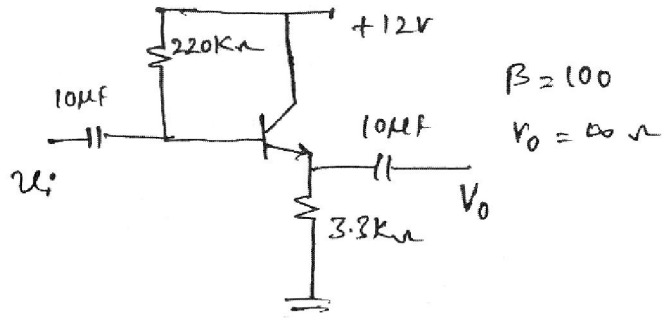


Fig.Q.3(b)

c. Prove that Miller effect of input capacitance $C_{Mi} = (1-A_v)C_f$ and output capacitance $C_{Mo} = \left(1 - \frac{1}{A_v}\right)C_f$. **(06 Marks)**

OR

4 a. For the following circuit determine Z_i, Z_o, A_v, A_i $h_{fb} = -0.99$, $h_{ib} = 14.3\Omega$. **(08 Marks)**

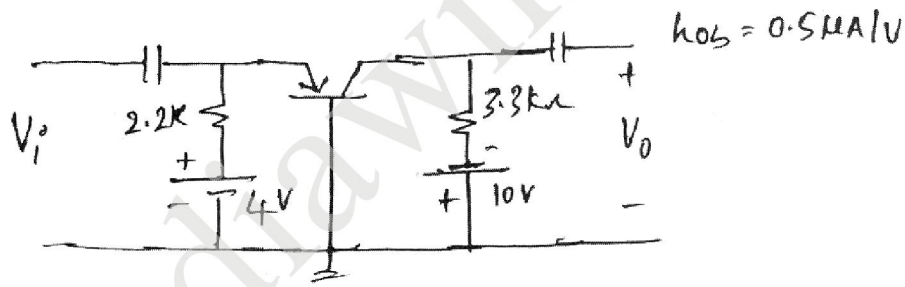


Fig.Q.4(a)

b. What are the advantages of h-parameters? **(06 Marks)**

c. Define h-parameters and obtain h-parameter equivalent circuit of CE configuration. **(06 Marks)**

Module-3

5 a. Obtain expression for voltage gain, current gain, input and output impedance of a Darlington Emitter follower circuit. Draw necessary equivalent circuit. **(12 Marks)**

b. With a neat block diagram, obtain expression for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

OR

6 a. Explain the general characteristics of negative feedback amplifier. **(08 Marks)**

b. Explain the need of cascading amplifier. A given amplifier arrangement has the following gains. $Av_1 = 10$, $Av_2 = 20$ and $Av_3 = 40$. Calculate overall voltage gain and total voltage gain in dB. **(06 Marks)**

c. With a simple block diagram, explain the concept of feedback amplifier. **(06 Marks)**

Module-4

7 a. With a neat circuit diagram, explain the operation of a class B push pull power amplifier and maximum conversion efficiency is 78.5%. **(08 Marks)**

b. With a neat circuit diagram, explain the operation of RC-phase shift oscillator using BJT and write f_{osc} equation. **(06 Marks)**

c. A series fed class A amplifier as shown in Fig.Q.7(c). Operates from a DC source and applied sinusoidal input signal generates peak base current 9mA. Calculate I_{CQ}, V_{CEQ}, P_{dc}, P_{ac} and efficiency. **(06 Marks)**

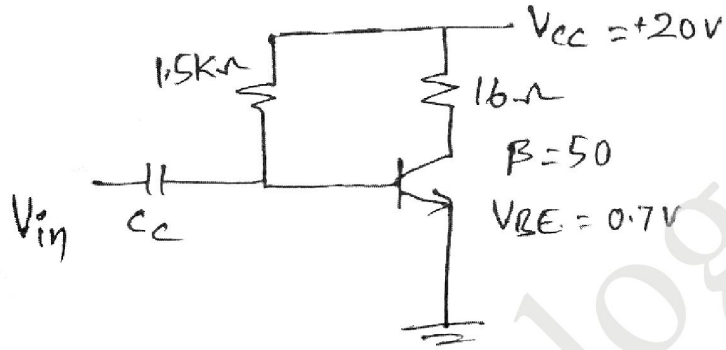


Fig.Q.7(c)

OR

8 a. The frequency selective circuit arms of wein bridge oscillator uses $C_1 = C_2 = 0.001\mu F$, $R_1 = 10K\Omega$ while R_2 is kept variable. The frequency is to be varied from 10Hz to 50kHz by varying R_2. Find the range of R_2. **(06 Marks)**

b. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier and prove that conversion efficiency is 50%. **(08 Marks)**

c. With a neat circuit diagram, explain the working principle of crystal oscillator in series resonant mode. **(06 Marks)**

Module-5

9 a. Explain the operation of JFET amplifier using fixed bias. Draw the JFET small signal model and derive the expression for Z_i, Z_o and A_v. **(06 Marks)**

b. Explain the construction, working and characteristics of n-channel enhancement type MOSFET. **(08 Marks)**

c. Determine the following for network shown in Fig.Q.9(c) V_{GSQ}, V_{DS}, V_S, V_G, V_D. **(06 Marks)**

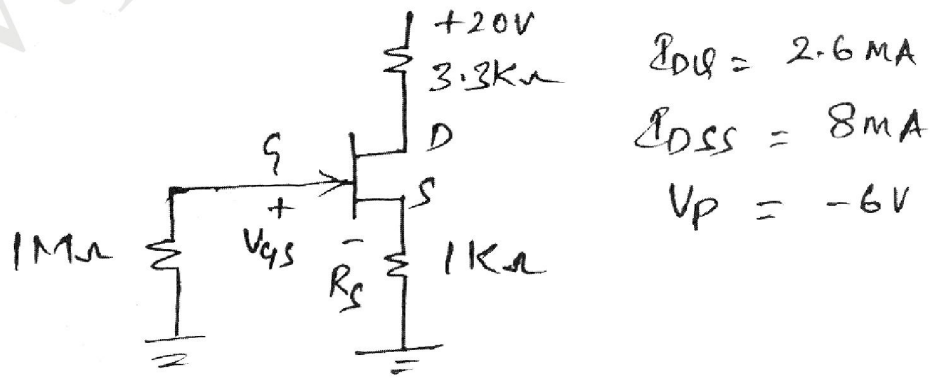


Fig.Q.9(c)

OR

10 a. Compare FET over BJT. **(06 Marks)**

b. With a neat diagrams, Explain the construction, working and characteristics of n-JFET's. **(08 Marks)**

c. Design the fixed bias network as shown in Fig.Q.10(c) having an a.c. gain of 10. Determine the value of R_D. **(06 Marks)**

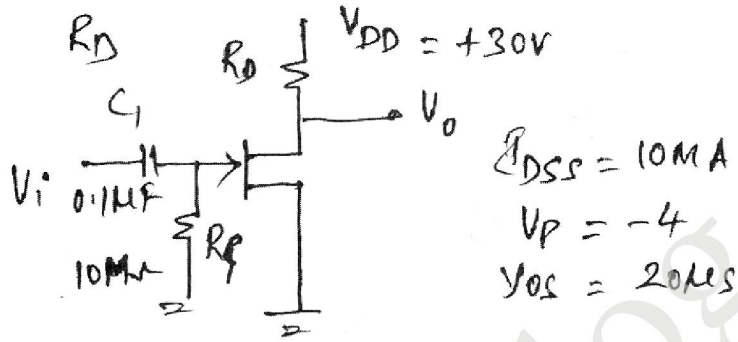


Fig.Q.10(c)

ADICHUNCHANAGIRI UNIVERSITY

18EC32

Third Semester BE Degree Examination March 2021
(CBCS Scheme)

Time: 3 Hours Max Marks: 100 marks

Sub: Analog Electronics

Q P Code: 62302

Instructions: 1. Answer **five full** questions.
2. Choose one full question from each module.
3. Your answer should be specific to the questions asked.
4. write the same question numbers as they appear in this question paper.
5. Write Legibly

Module – 1

1	a	Compare the characteristics of CB,CC and CE configuration with necessary circuits and represent them in re model.	10 marks
	b	What is transistor biasing? Explain the fixed bias circuit with relevant equations and circuit	10 marks

Or

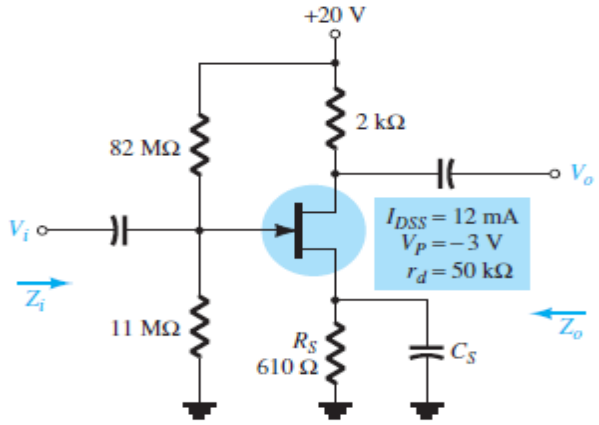
2	a	Derive an expression for Av,Zi, Zo for emitter follower circuit using re model.	10 marks
	b	Determine the values of R1 and Rc for voltage divider bias circuit with Vcc=20V ,R2=22 KΩ ,R_E=1 KΩ and I_C=2.5mA	10 marks

Module – 2

3	a	Explain low frequency response of FET amplifier and derive an expression for cut off frequencies defined by input and output circuits.	10 marks
	b	Determine the lower cut off frequency for the FET amplifier using the following parameters C_G=0.01µF,C_C=0.5 µF,C_S=2 µF Rsig=10KΩ , R_G=1MΩ, R_D=4.7KΩ,Rs=1KΩ,R_L=2.2KΩ, I_{DSS}=8mA,Vp=**-4v**$r_{d=}$∞Ω,V_{DD}=20V,V_{GSQ}=-2V,I_{DQ}=2mA	10 marks

Or

4	a	Derive an expression for Zi and Zo, Av for common gate configuration for JFET.	10 marks
	b	For JFET voltage divider bias calculate Zi, Zo and Av and also find Vo if Vi=25mV(rms)	10 marks



PTO

Module – 3

5	a	Consider common drain amplifier circuit with gm=1m A/V and ro=150 KΩ let Rsig=1 MΩ and R_L=15 KΩ find Rin, Rout ,Av and Gv	10 marks
	b	From small signal operation of an amplifier derive an expression for DC bias point, signal current in Drain terminal (i_D), voltage gain and trans conductance	10 marks

Or

6	a	Explain CS amplifier with necessary circuit and equations with and without source resistance	10 marks
	b	Explain the different types of internal capacitances in MOSFET and explain the gate capacitive effect.	10 marks

Module – 4

7	a	For a voltage series feedback amplifier topology. Obtain an expression for Av, Rif and Rof.	10 marks
	b	A crystal oscillator has L=0.334H, C=0.065pF,C_M=1pF,R=5.5KΩ calculate its series and parallel resonating frequency and find Q of the crystal	10 marks

Or

8	a	Briefly explain Barkhausen criterion for oscillations and explain RC phase shift oscillator with necessary circuit and equations	10 marks
	b	With neat circuit diagram explain the operation of BJT colpitts oscillator.	10 marks

Module – 5

9	a	With neat circuit diagram, explain the operation of a transformer coupled class A power amplifier.	10 marks
	b	Derive an expression for second harmonic distortion in power amplifier using 3-point method.	10 marks

Or

10	a	With neat circuit diagram explain the operation of a class B push pull power amplifier and derive its conversion efficiency..	10 marks
	b	Briefly explain series voltage regulator and shunt voltage regulator with necessary block diagrams.	10 marks

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Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive an expression for S_{Ico} and S_{VB} of collector to base bias circuit. **(08 Marks)**

b. Design a suitable Clipper circuit to the output shown in Fig Q1(b). Assume silicon diode.

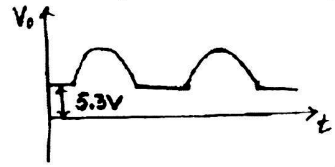


Fig Q1(b) **(05 Marks)**

c. Find I_c, V_E, V_B, V_C and V_{CE} for the circuit shown in Fig 1(c). Assume silicon transistor with $\beta = 60$.

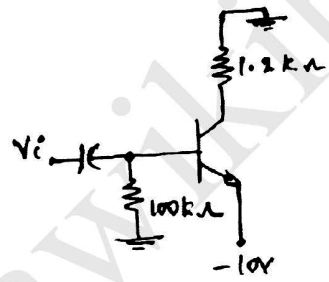


Fig Q1(c) **(07 Marks)**

OR

2 a. Explain how a transistor can be used as a switch. **(07 Marks)**

b. Determine I_E, I_B, V_{CE}, V_{CB}, V_C, and V_E for the network shown in Fig Q2(b). Assume silicon transistor with $\beta = 60$.

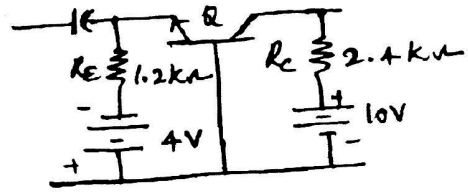


Fig Q2(b) **(07 Marks)**

c. Determine V_o for the network shown in Fig Q2(c) the frequency of i/p signal is 1KHz. Assume ideal diode.

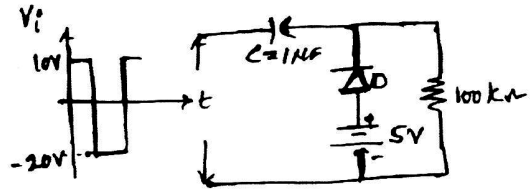


Fig Q2(c) **(06 Marks)**

Module-2

3 a. For the network shown in Fig Q3(a) determine z_i, z_o, A_v and A_I

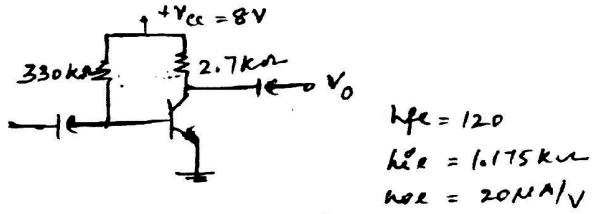


Fig Q3(a) **(08 Marks)**

b. Derive an expression for z_i, z_o, A_v for emitter follower configuration using approximate hybrid model. **(08 Marks)**

c. Obtain the expression for Miller i/p capacitance. **(04 Marks)**

OR

4 a. Draw the complete hybrid equivalent model of a transistor. Derive an expression for z_i, z_o, A_I and A_v. **(10 Marks)**

b. For the common base amplifier shown in Fig Q4(b), determine: i) z_i ii) A_I iii) A_V. Give hie = 1.6kΩ, hfe = 110, hre = 2×10^{-4}, hoe = 20μA/v.

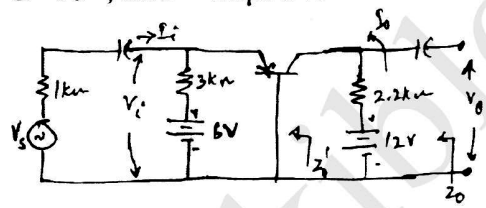


Fig Q4(b) **(10 Marks)**

Module-3

5 a. For the Darlington emitter, follower shown in Fig Q5(a)

i) Calculate the dc bias voltages V_B, V_E, V_c and currents I_B and I_C

ii) Calculate the i/p and o/p impedances

iii) Determine the voltage and current gains

iv) The ac o/p voltage for V_i = 120mV.

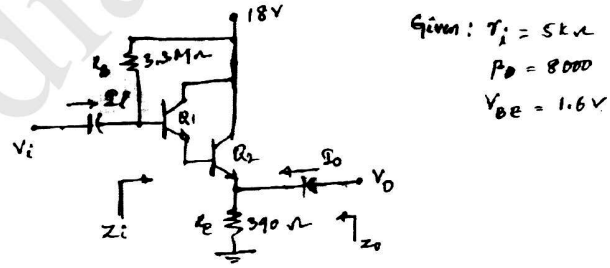


Fig Q5(a) **(10 Marks)**

b. For the cascaded arrangement shown in Fig Q5(b), calculate :

i) The loaded voltage gain of each stage

ii) The total gain of the system A_V and A_{VI}

iii) The loaded current gain of each stage

iv) The total current gain of the system.

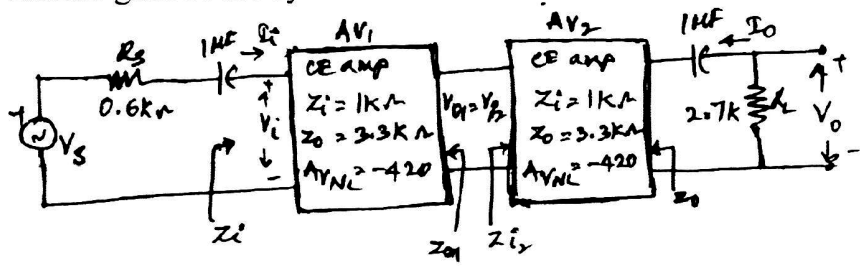


Fig Q5(b) **(10 Marks)**

OR

6 a. List the advantages of negative feedback. **(10 Marks)**

b. Derive an expression for input resistance of current series and current shunt feedback amplifier. **(04 Marks)**

c. Negative feedback to be used to reduce noise from an amplifier by 90% i) what mast the percentage negative feedback to accomplish this, if the initial voltage gain is 50?
ii) What will be the voltage gain with feedback. **(06 Marks)**

Module-4

7 a. Derive an expression for frequency of oscillation of RC phase shift oscillator. **(10 Marks)**

b. With a neat circuit diagram, explain the working of complementary class B power amplifier. **(06 Marks)**

c. The following distortion readings are available for a power amplifier. $D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$ with $I_1 = 3.3$ A and $R_C = 4\Omega$.
i) Calculate THD ii) Determine the fundamental power iii) calculate the total power **(04 Marks)**

OR

8 a. With a neat circuit diagram, explain the working of Hartley oscillator. **(06 Marks)**

b. For a class B amplifier providing a 20V peak signal to a 16Ω load and a power supply of $V_{CC} = 30V$, determine the i/p power, o/p power and efficiency. **(06 Marks)**

c. Explain the classification of power amplifier based on Q- point. **(08 Marks)**

Module-5

9 a. Draw the circuit a fixed bias JFET amplifier and its equivalent circuit. Hence obtain the expression Z_{in}, Z_0 and A_V. **(10 Marks)**

b. A JFET has device parameter of $g_{mo} = 10m\mho$ and $I_{DSS} = 12mA$. When the device is suitably biased, the drain current was found to be 8mA. Determine : i) V_P ii) g_m iii) V_{GS} **(06 Marks)**

c. Give the comparison of FET over BJT. **(04 Marks)**

OR

10 a. With a neat sketch, explain the construction and working principle of N-channel enhancement type MOSFET and also explain its static drain characteristics. **(10 Marks)**

b. Obtain the expression for trans conductance g_m of JFET. **(04 Marks)**

c. For the voltage divider bias configuration shown in Fig Q10(c). Determine the value of R_s, if $V_D = 12V$ and $V_{GSQ} = -2V$.

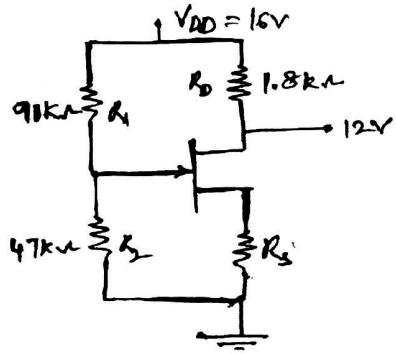


Fig Q10(c) **(06 Marks)**

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronics Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw a double ended clipper circuit and explain the working principle with transfer characteristics. **(10 Marks)**

b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero. **(10 Marks)**

OR

2 a. Derive the expression for stability factors S′ and S″ for fixed bias circuit. **(08 Marks)**

b. A voltage divider biased circuit has $R_1 = 39K\Omega$, $R_2 = 82K\Omega$, $R_C = 3.3K\Omega$, $R_E = 1K\Omega$ and $V_{CC} = 18V$. The silicon transistor used has $\beta = 120$. Find Q-point and stability factor. **(07 Marks)**

c. Explain the operation of transistor as switch with suitable circuit and necessary waveforms. **(05 Marks)**

Module-2

3 a. State and prove Millers theorem. **(06 Marks)**

b. Compare the characteristics of CB, CE and CC configurations. **(06 Marks)**

c. For the collector feedback configuration having $R_F = 180K\Omega$, $R_C = 2.7K\Omega$, $C_1 = 10\mu F$, $C_2 = 10\mu F$, $\beta = 200$, $r_0 = \infty\Omega$ and $V_{CC} = 9$volts. Determine the following parameters:
i) re ii) z_i iii) z_o iv) A_v **(08 Marks)**

OR

4 a. Derive suitable expression to explain the effect of cascading of amplifiers on lower and upper cut off frequencies. **(08 Marks)**

b. Derive equations for miller input capacitance and miller output capacitance. **(08 Marks)**

c. A transistor in CE mode has h-parameters $h_{ie} = 1.1K\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. **(04 Marks)**

Module-3

5 a. Derive expression for Zi and Ai for a Darlington Emitter follower circuit. **(10 Marks)**

b. Explain the need of a cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier. **(06 Marks)**

c. Write a note on cascade amplifier. **(04 Marks)**

OR

6 a. List the general characteristics of negative feedback amplifier. **(04 Marks)**

b. A given amplifier arrangement has the following voltage gain $AV_1 = 10$, $AV_2 = 20$ and $AV_3 = 40$. Calculate the overall voltage gain and determine the total voltage gain in dBS. **(08 Marks)**

c. For the voltage series feedback amplifier. Derive an expression for output impedance (Resistance). **(08 Marks)**

Module-4

7 a. Show that maximum efficiency of class-B push pull amplifier (power amplifier) circuit is 78.54%. **(08 Marks)**

b. Explain the classification of power amplifier with a neat circuit diagram and waveforms. **(07 Marks)**

c. A class-B push pull amplifier operating with $V_{CC} = 25V$ provides a 22V peak signal to 8Ω load. Calculate the circuit efficiency and power dissipated per transistor. **(05 Marks)**

OR

8 a. Draw the circuit of wein bridge oscillator and explain its operation. **(10 Marks)**

b. With a neat circuit diagram and waveform, explain the working principal of crystal oscillator operating in series resonant mode. A crystal has the following parameters L = 0.334H, C = 0.065pF and R = 5.5KΩ. Calculate its resonant frequency. **(10 Marks)**

Module-5

9 a. With the help of neat diagram, explain the working and characteristics of N-channel JFET. **(10 Marks)**

b. For a self bias JFET circuit, $V_{DD} = +12V$, $R_D = 2.2K\Omega$, $R_G = 1M\Omega$, $R_S = 1K\Omega$, $I_{DSS} = 8mA$, $V_P = -4$ Volts. Determine the following parameters: i)V_{GS} ii) I_D iii) V_{DS} iv) V_S v) V_G vi) V_D **(10 Marks)**

OR

10 a. With neat sketches, explain the operation and characteristics of n-channel depletion type MOSFET. **(10 Marks)**

b. Derive expression for V_{GS}, I_D, V_{DS}, V_D and V_S for a voltage divider bias circuit using FET. **(10 Marks)**

ADICHUNCHANAGIRI UNIVERSITY

18EC32

Third Semester BE Degree Examination January 2020

(CBCS Scheme)

Time: 3 Hours Max Marks: 100 Marks

Sub: ANALOG ELECTRONICS

Instructions:
1. Answer five full questions
2. Choose one full question from each module
3. Your answer should be specific to the questions asked
4. Write the same question numbers as they appear in this question paper
5. Write Legibly.

Module -1

1	a	Define h-parameter. Draw the h-parameter model of a CE configuration.	10	M
	b	Derive an expression for I_B, I_C and V_{CE} for voltage divider bias using exact analysis.	10	M

Or

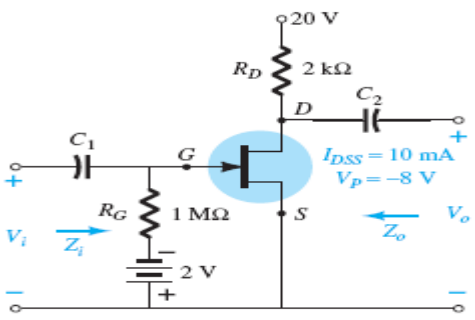
2	a	Derive an expression for Av, Zi, Zo for Emitter follower using re model	10	M
	b	A voltage divider biased circuit has Rc=4KΩ, R_E=1.5KΩ, R_1=39KΩ, R2=3.9KΩ Vcc=18V and β=70. Find Ic,$V_{CE.}$	10	M

Module -2

3	a	Explain high frequency response of FET amplifier and derive an expression for cut off frequencies defined by input and output circuits.	10	M
	b	Determine the lower cut off frequency for the FET amplifier using the following parameters C_G=0.01μF,C_C=0.5 μF,C_S=2 μF Rsig=10KΩ , R_G=1MΩ, R_D=4.7KΩ,Rs=1KΩ,R_L=2.2KΩ, I_{DSS}=8mA,Vp=-4v $r_{d=}$∞Ω,V_{DD}=20V,V_{GSQ}=-2V,I_{DQ}=2mA	10	M

Or

4	a	Derive an expression for Zi and Zo, Av for self-bias configuration for JFET.	10	M
	b	The fixed-bias configuration of FET amplifier had an operating point defined by V_{GSQ} = -2 V and I_{DQ} = 5.625 mA, with I_{DSS} = 10 mA and VP = -8 V. The network is shown below with an applied signal Vi Yos=40μS.	10	M



Module -3

5	a	Explain CS amplifier with necessary circuit and equations with and without source resistance	12	M
	b	From small signal operation of an amplifier derive an expression for DC bias point, signal current in Drain terminal (i_D), voltage gain and trans conductance	08	M

Or

6	a	With neat diagram and small signal model of common drain amplifier prove that Avo=1,Gv=1	10	M
	b	Explain the different types of internal capacitances in MOSFET and explain the gate capacitive effect.	10	M

Module -4

7	a	For a voltage series feedback amplifier topology. obtain an expression for Av, Rif and Rof also explain the practical feedback circuit using voltage series feedback.	10	M
	b	with neat circuit diagram explain the working of series resonant crystal oscillator.A crystal oscillator has L=0.334H, C=0.065pF,C_M=1pF,R=5.5KΩ calculate its series and parallel resonating frequency.	10	M

Or

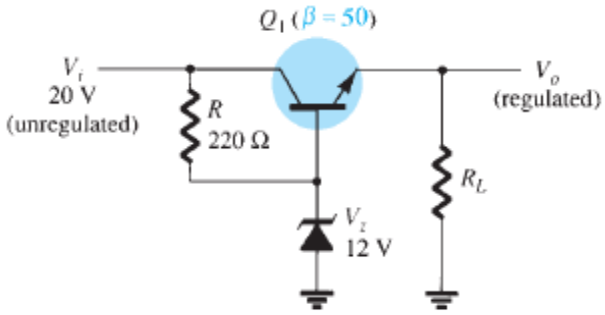
8	a	What are tuned oscillators? Explain the two types of tuned oscillators.	10	M
	b	Briefly explain Barkhausen criterion for oscillations and explain RC phase shift oscillator with necessary circuit and equations.	10	M

Module -5

9	a	Explain the working of class B push pull power amplifier. Derive an expression for its efficiency S T η=78.4%	10	M
	b	Derive an expression for second harmonic distortion in power amplifier using 3-point method.	10	M

Or

10	a	With neat circuit diagram explain the operation of a series-fed class A power amplifier and prove that η=25%.	10	M
	b	Briefly explain the series voltage regulator. Calculate the output voltage and the Zener current in the regulator circuit of Figure shown below for R_L = 1KΩ	10	M



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